WHAT IS CLAIMED IS:

1. A method of forming a multilayered circuit board, comprising:

a first circuit forming process of forming a first circuit made of a conductor in a predetermined pattern on a first flat surface of a flat insulating board made of an insulating material, the insulating board further having a second flat surface approximately parallel to the first flat surface;

a first circuit embedding process of embedding the first circuit in the first insulating board so that the first surface and the first circuit have a predetermined surface flatness and that the first surface has a predetermined parallelism with respect to the second flat surface;

a masking process of forming, on a part of a surface of the embedded first circuit, a mask for forming a pilot hole for a via hole;

an insulating layer forming process of forming an insulating material layer by applying the insulating material as a layer to the first flat surface having the mask formed thereon except the part of the surface on which the mask is located;

an insulating material layer flattening process of flattening a surface of the insulating material layer so that the surface of the insulating material layer has the surface flatness and the parallelism with respect to the second flat surface; and

a pilot hole forming process of forming the pilot hole by removing the mask from the first circuit with the insulating material layer being flattened.

2. The method of forming the multilayered circuit board according to claim 1, wherein

$S < 5\mu m$, and

$P < 5\mu m$,

where S is the surface flatness and P is the parallelism.

3. The method of forming the multilayered circuit board according to claim 1, wherein

the first circuit embedding process includes:

a process of heating and maintaining the insulating material and the first circuit at a predetermined temperature T; and

a process of pressuring the heated and maintained insulating material and first circuit at a predetermined pressure F to the second flat surface with the surface flatness and the parallelism, wherein

$100℃ \leqq T \leqq 200℃$,

$2\times10^6Pa \leqq F \leqq 5\times10^6Pa$, and

$300\times10^6Pa \leqq T\times F \leqq 600\times10^6Pa$.

4. The method of forming the multilayered circuit board

according to claim 1, further comprising:

a via hole forming process of forming the via hole by filling the pilot hole with the conductor;

a second circuit forming process of forming a second circuit by applying the conductor to the surface of the flattened insulating material layer in a predetermined pattern; and

a second circuit embedding process for embedding the second circuit in the flattened insulating material layer so that the surface of the flattened insulating material layer and the second circuit have the surface flatness and that the surface of the flattened insulating material layer has the parallelism with respect to the second flat surface.

5. The method of forming the multilayered circuit board according to claim 4, further comprising

a circuit board multilayering process of successively forming a predetermined number of circuit boards by repeating the second circuit forming process and the second circuit embedding process for a predetermined number of times.

6. The method of forming the multilayered circuit board according to claim 1, wherein

the insulating material contains a plastic component.

7. The method of forming the multilayered circuit board

according to claim 1, wherein

the conductor is selected from a group including Au, Ag, Cu, Ni, Sn, and Pd.

8. The method of forming the multilayered circuit board according to claim 1, wherein

the conductor is selected from a group including a Au compound, a Ag compound, a Cu compound, a Ni compound, a Sn compound, and a Pd compound.

9. The method of forming the multilayered circuit board according to claim 1, wherein

the conductor is selected from a group including an alloy mainly containing any of Au, Ag, Cu, Ni, Sn, and Pd.

10. The method of forming the multilayered circuit board according to claim 1, wherein

the conductor is a mixture of an alloy mainly containing any of Au, Ag, Cu, Ni, Sn, and Pd, and an organic compound.

11. The method of forming the multilayered circuit board according to claim 1, wherein

the mask is selected from a group including a compound containing fluorine, a monad, a resin, a polyethylene resin, a polypropylene resin, a vinyl chloride resin, a nylon resin, a

sublime compound, and a basic acid compound.

12. The method of forming the multilayered circuit board according to claim 1, wherein

the mask is formed through any of plasma coating, PVD, CVD, PCVD, spraying, and printing.

13. The method of forming the multilayered circuit board according to claim 1, wherein

the mask is removed through a scheme selected from a group including plasma etching, spattering, chemical etching, and heating.

14. The method of forming the multilayered circuit board according to claim 1, wherein

in the first circuit forming process, the first circuit includes a component.

15. The method of forming the multilayered circuit board according to claim 4, wherein

in the second circuit forming process, the second circuit includes a component.

16. A multilayered circuit board formed by using the method according to claim 1.

17. A multilayered circuit board formed by using the method according to claim 4.